

FIG. 1

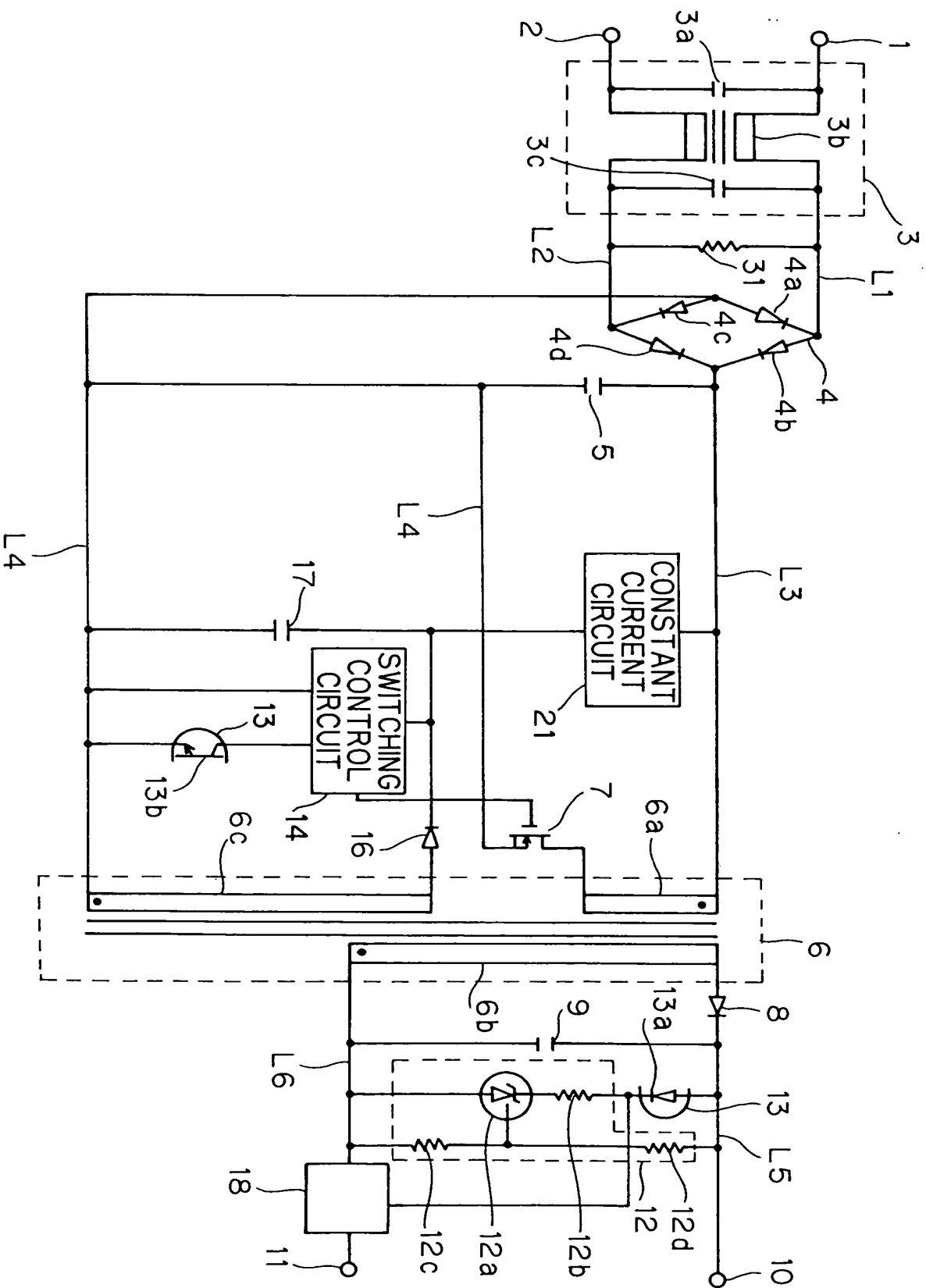
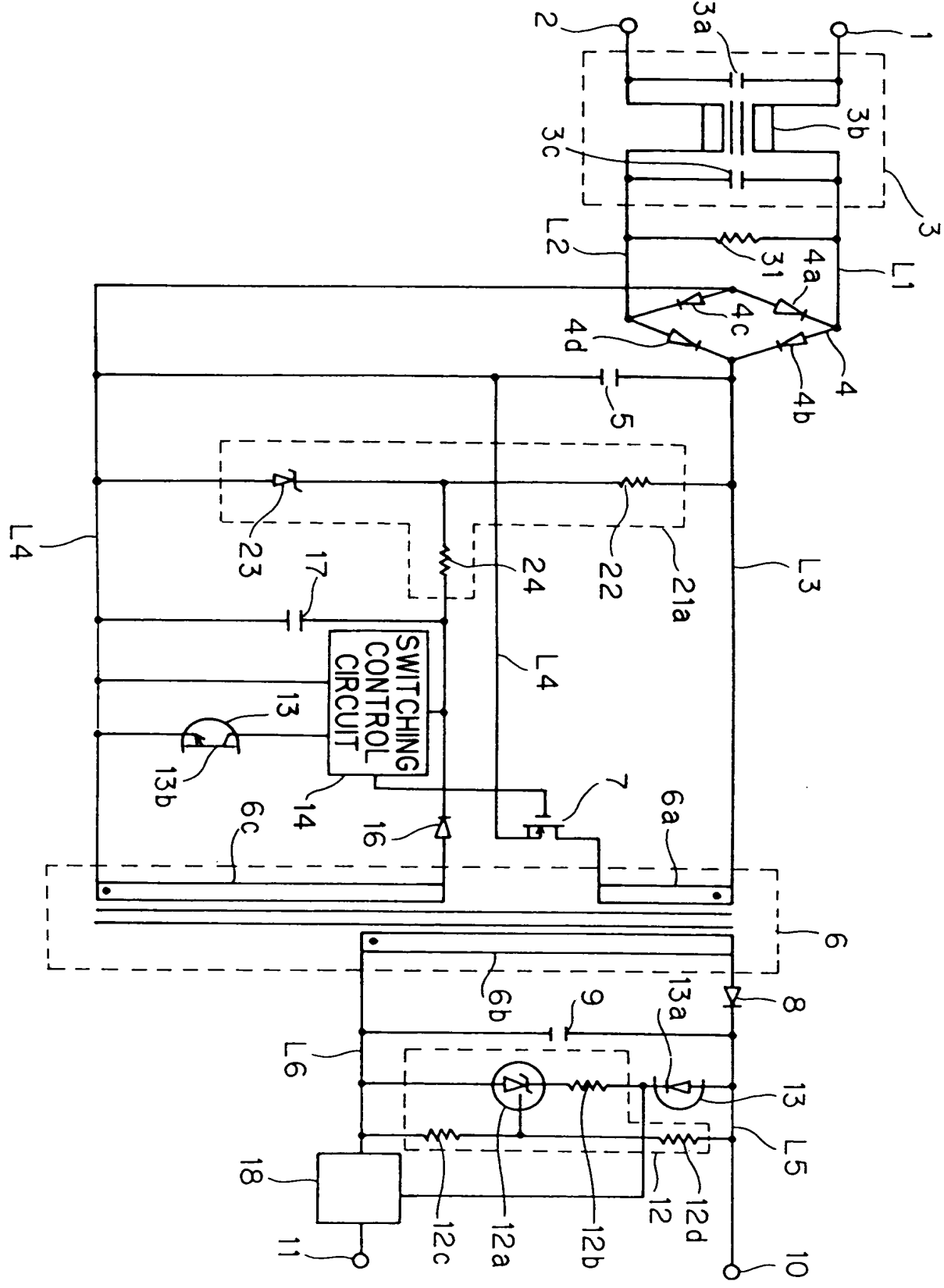


FIG. 2



The circuit diagram shows a differential amplifier. The input stage consists of two NMOS transistors, 3a and 3b, whose gates are connected to a common-mode input signal 1. The sources of 3a and 3b are connected to a common source node, which is connected to ground through a resistor 31. The drains of 3a and 3b are connected to a common drain node, which is connected to a supply voltage 2 through a resistor 3c. The output stage consists of two PMOS transistors, 4a and 4b, whose gates are connected to a common-mode input signal 1. The sources of 4a and 4b are connected to a common source node, which is connected to ground through a resistor 31. The drains of 4a and 4b are connected to a common drain node, which is connected to a supply voltage 2 through a resistor 3c. The output of the differential amplifier is taken from the common drain node, which is connected to a load resistor 4d. The output signal is labeled 4.

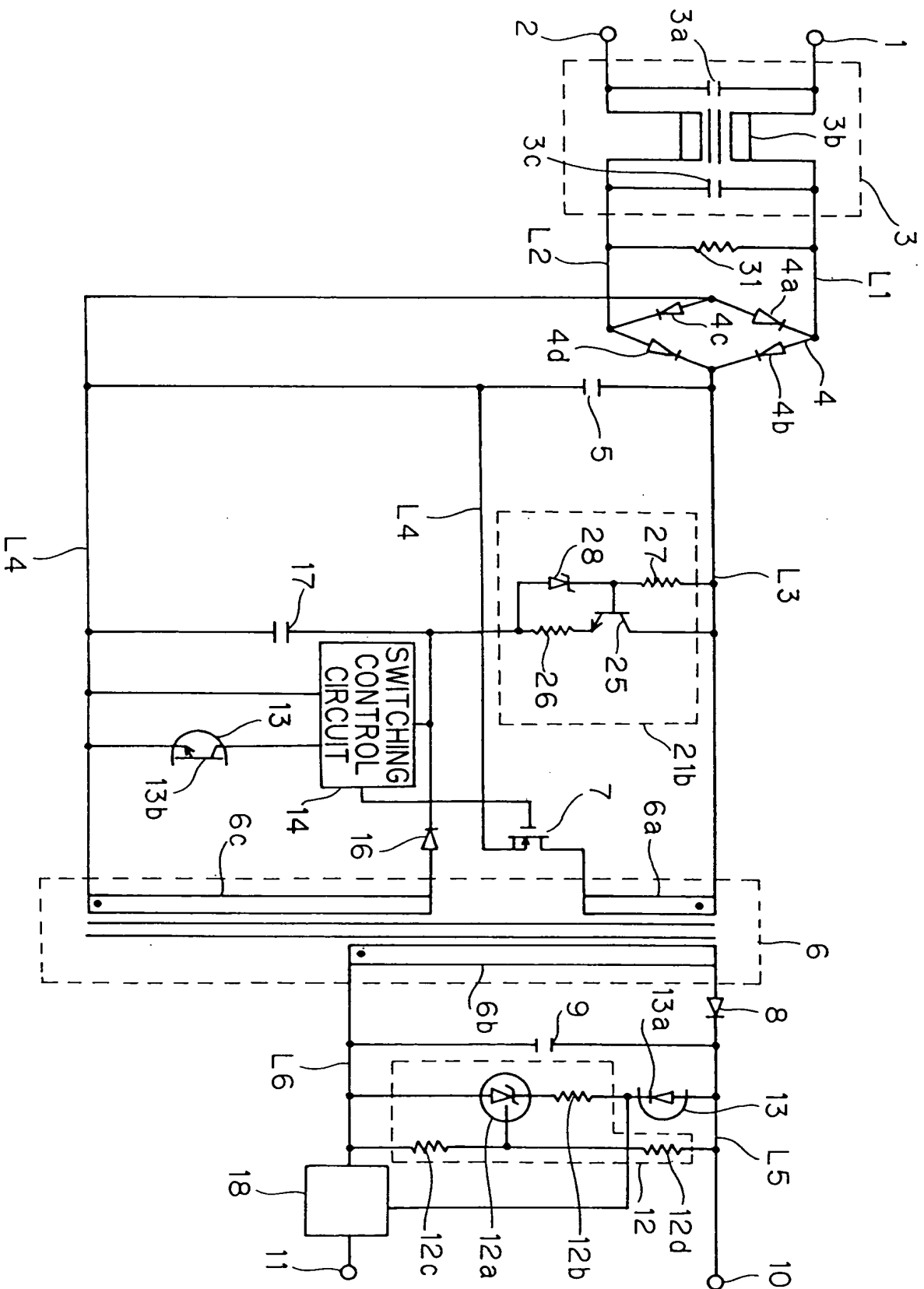


FIG. 4

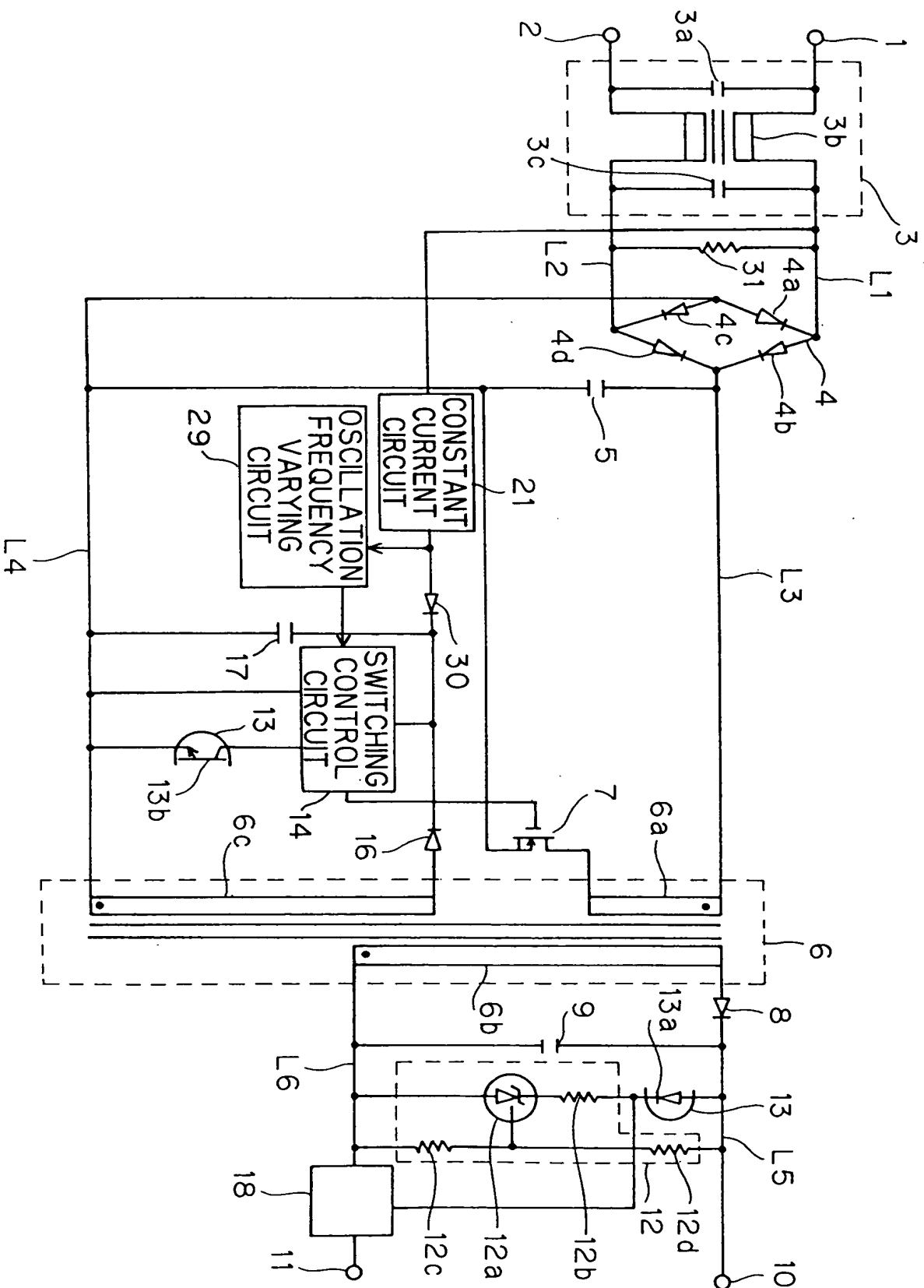
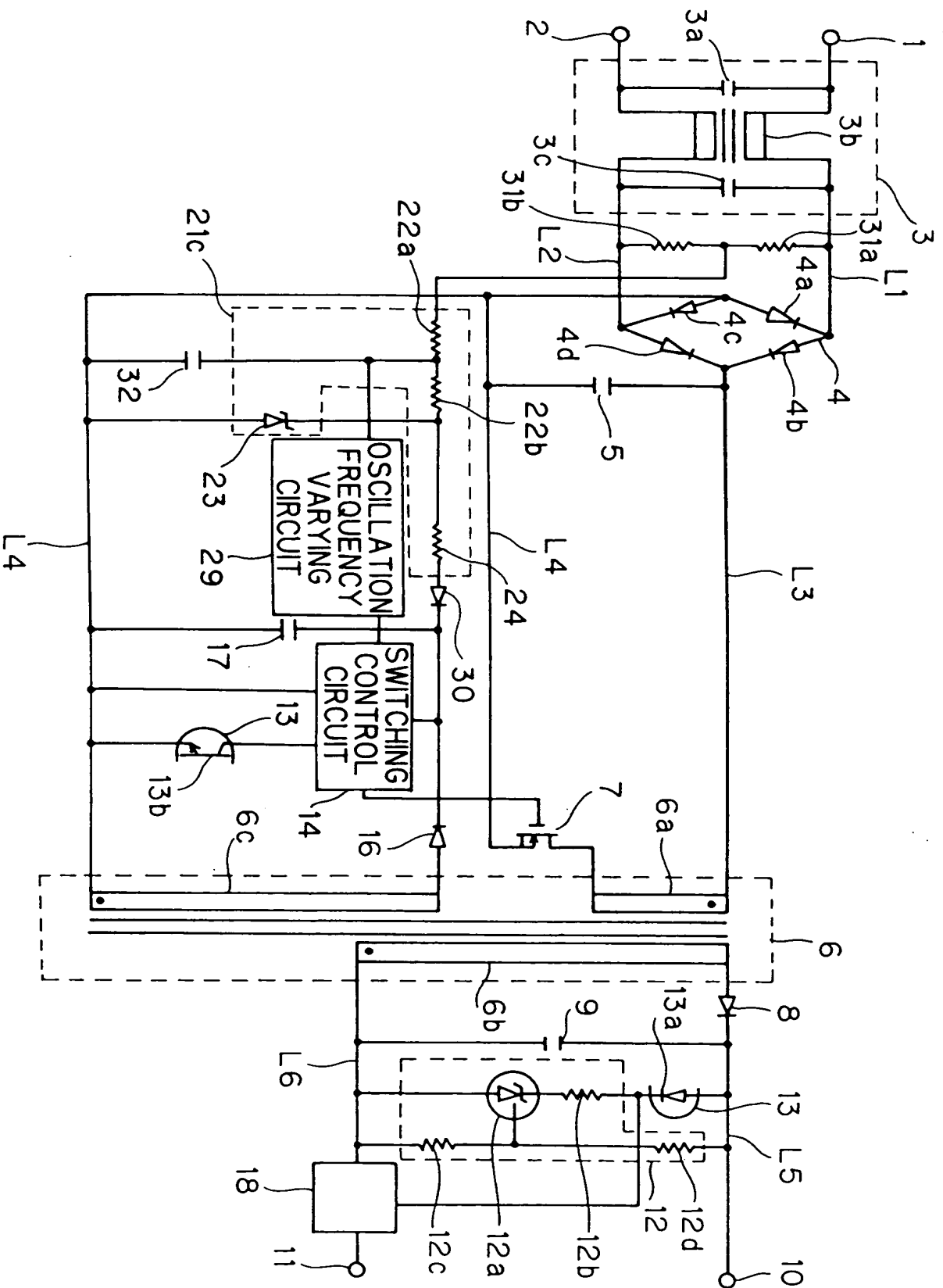
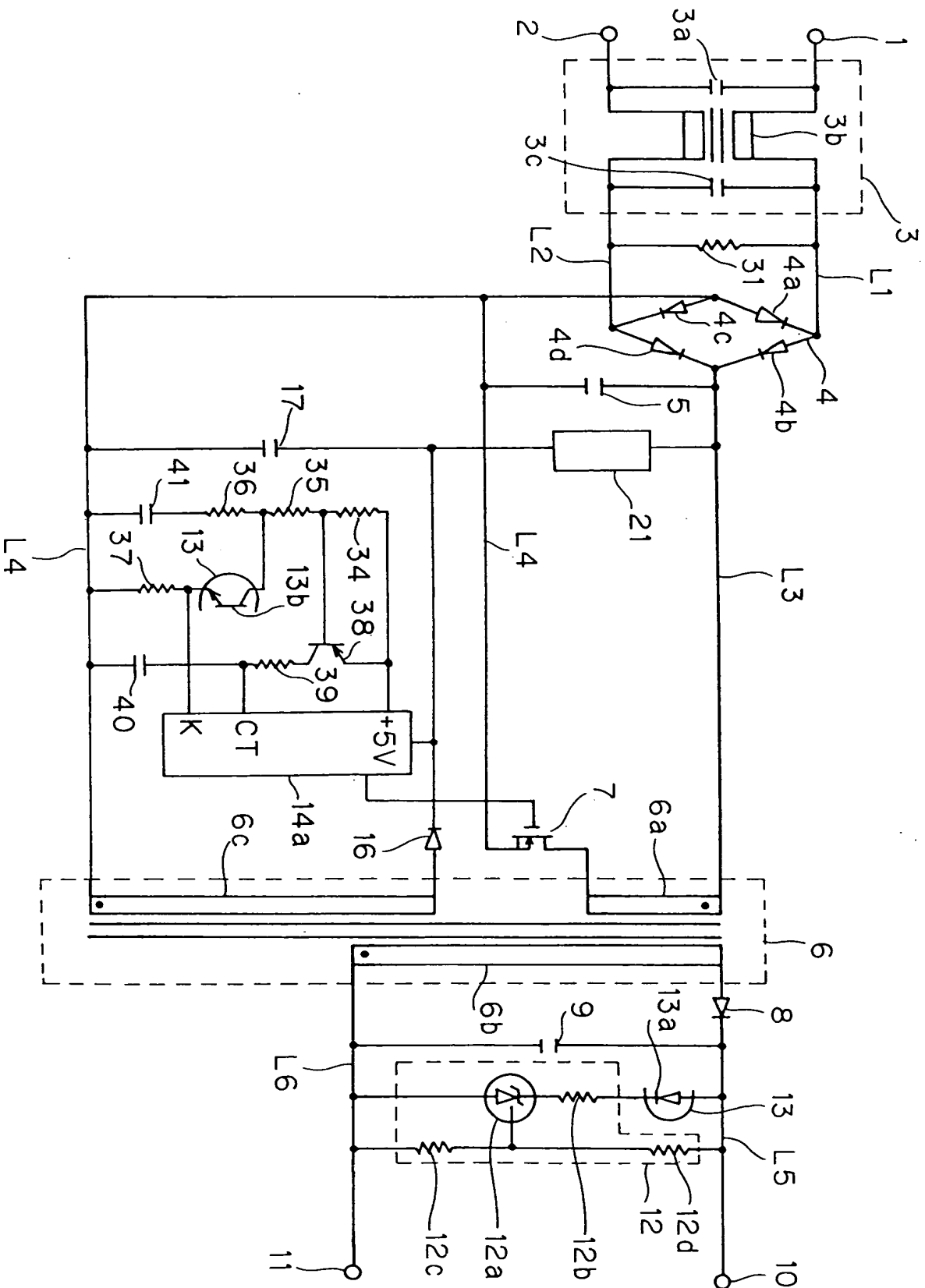


FIG. 5



The diagram illustrates a power supply system. It begins with an AC input (1) connected to a bridge rectifier (4) via a line L1. The rectifier's output is connected to a filter capacitor (3) through a line L2. A resistor (31) is also connected to the output of the rectifier. The output of the filter capacitor is connected to a switching regulator circuit (6) through a line L3. The switching regulator circuit includes a switching transistor (7) and a diode (8). The output of the switching regulator is connected to a load (10) through a line L5. The load is connected to ground (9) through a resistor (12). The switching regulator circuit also includes a diode (13a) and a resistor (12d).



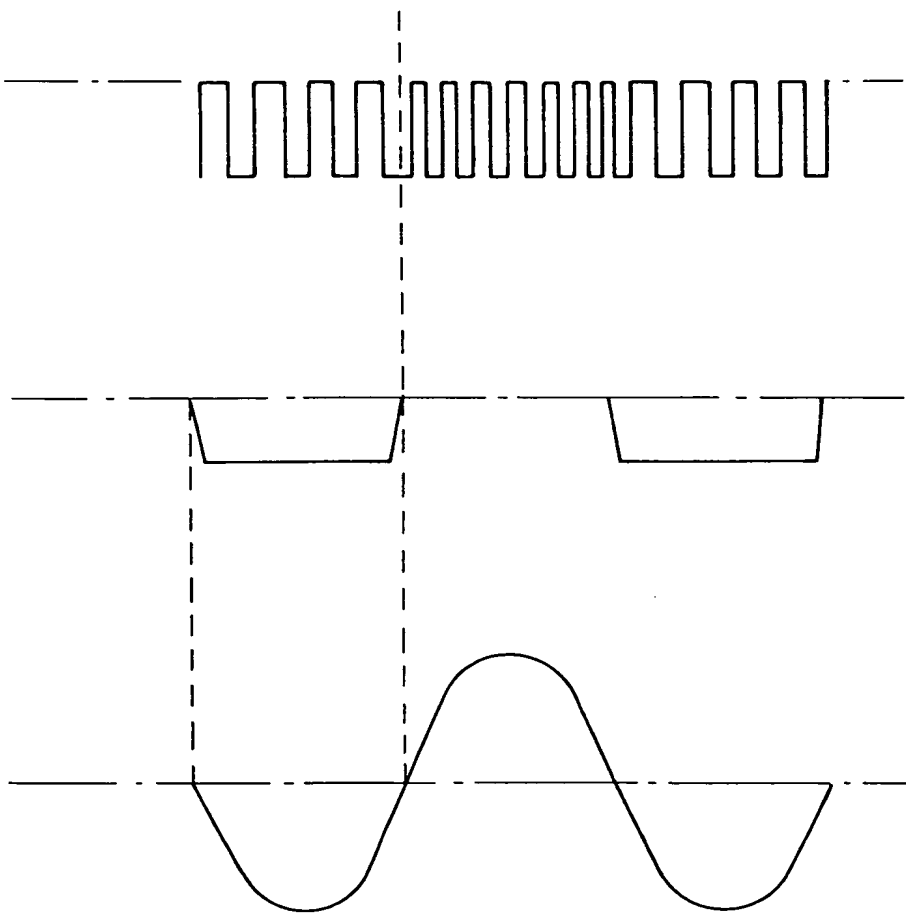


FIG. 7A

FIG. 7B

FIG. 7C

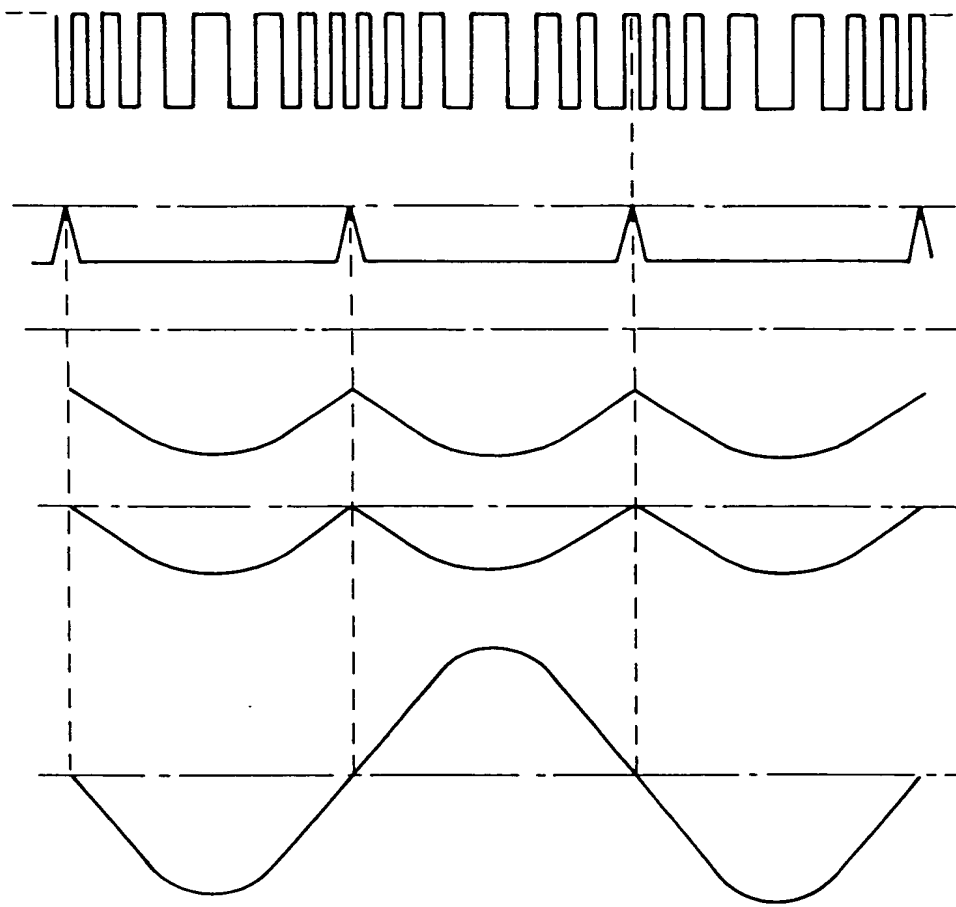


FIG. 8A

FIG. 8B

FIG. 8C

FIG. 8D

FIG. 8E

OPERATION
START
VOLTAGE
MINIMUM
OPERATING
VOLTAGE

FIG. 9A

FIG. 9B

FIG. 9C

FIG. 9D

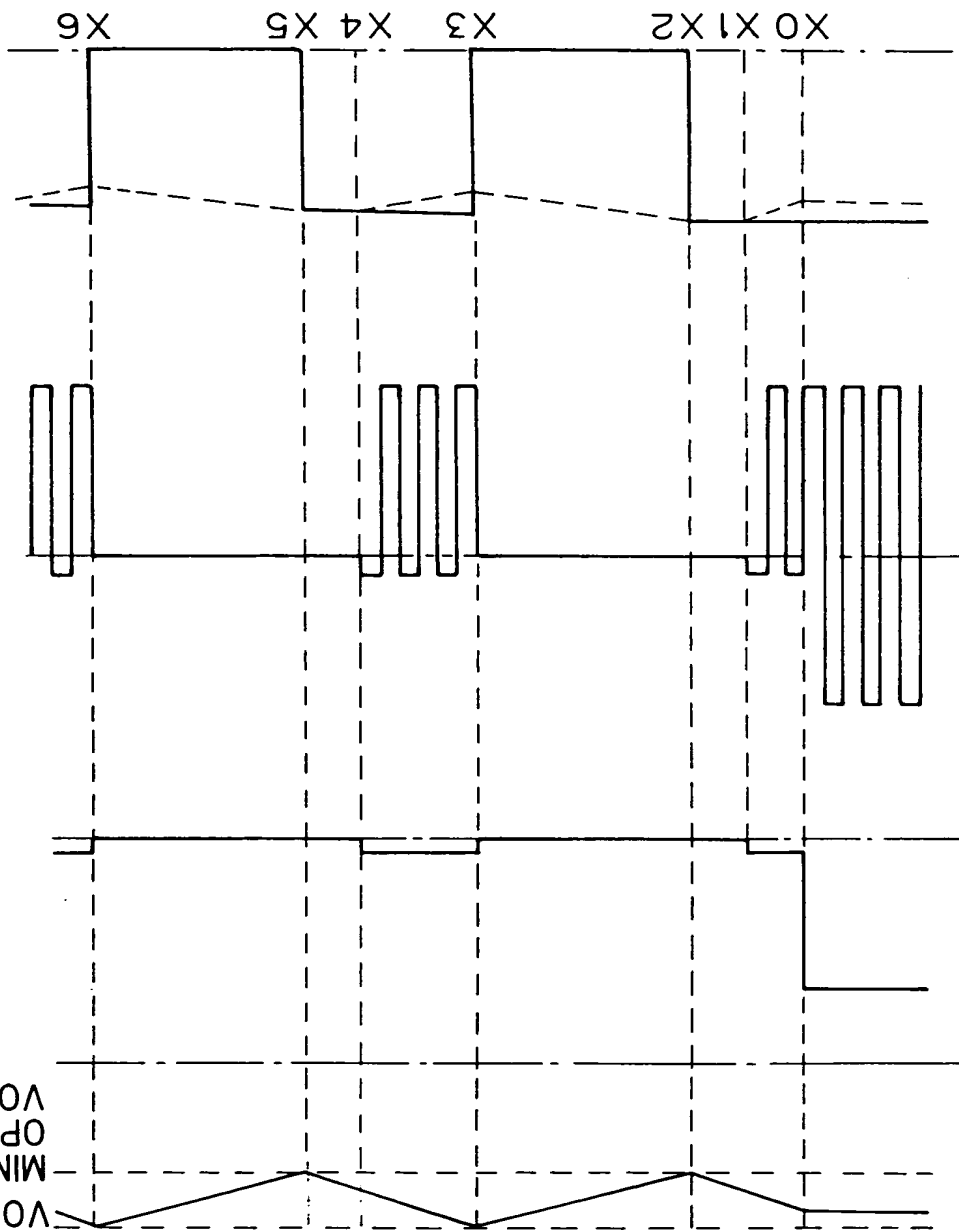


FIG. 10 PRIOR ART

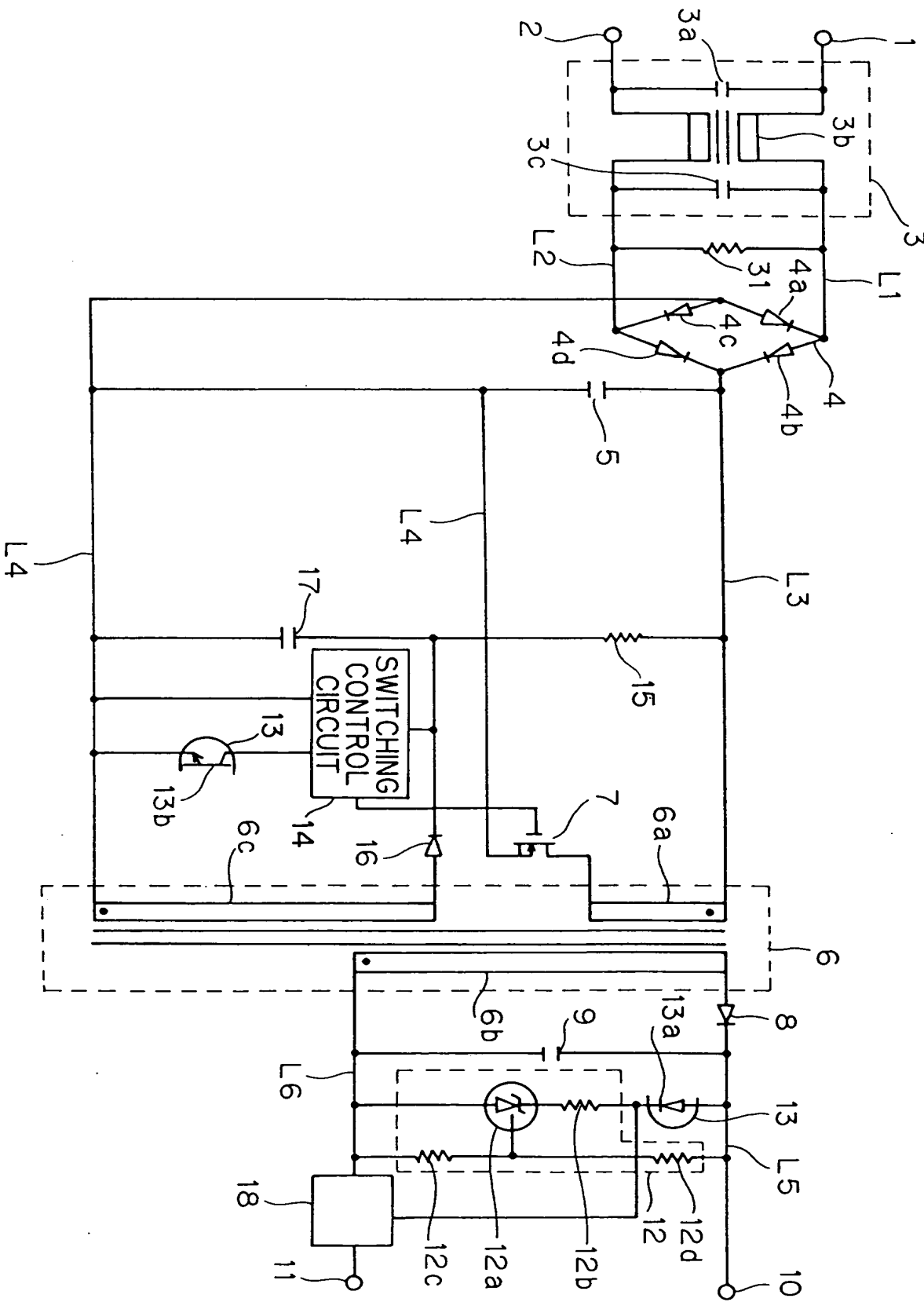


FIG. 11A
PRIOR ART

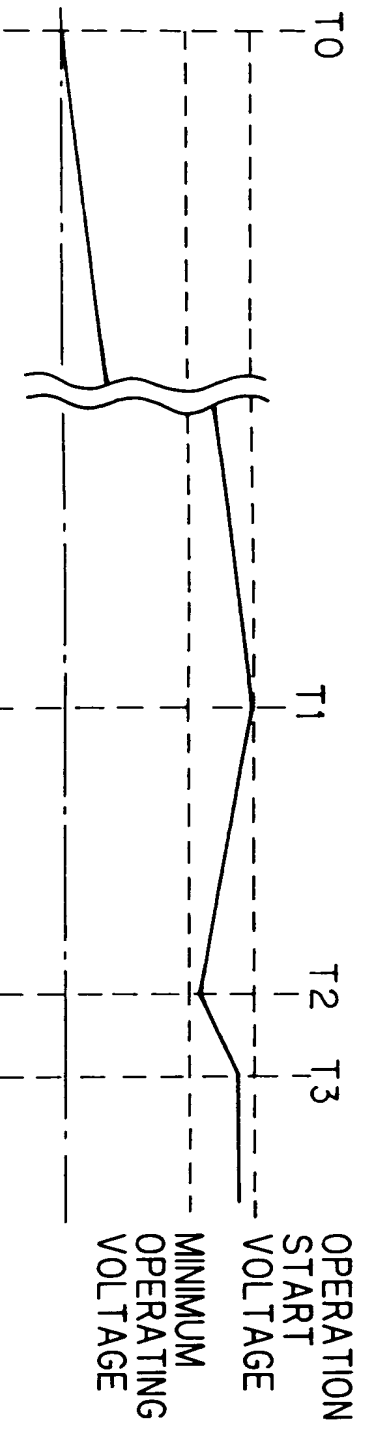


FIG. 11B
PRIOR ART

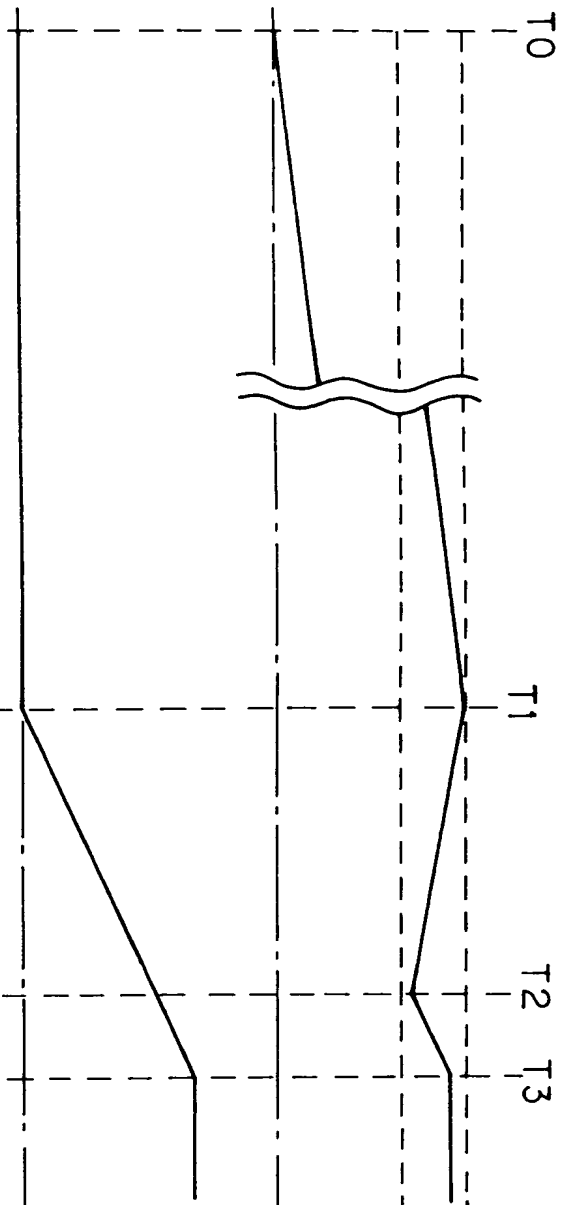
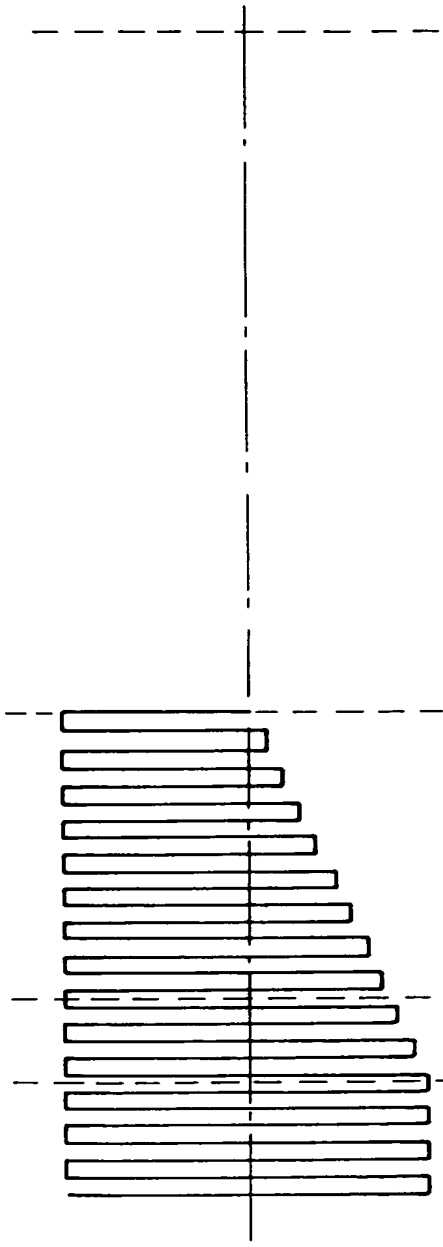


FIG. 11C
PRIOR ART



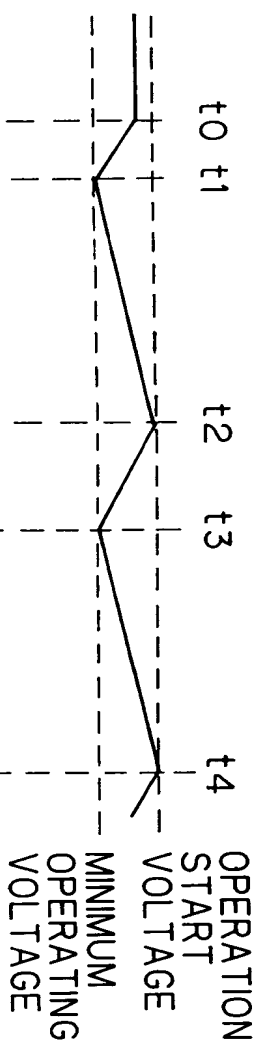


FIG. 12 A
PRIOR ART

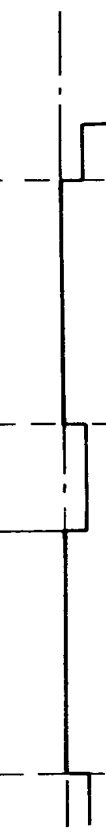


FIG. 12 B
PRIOR ART

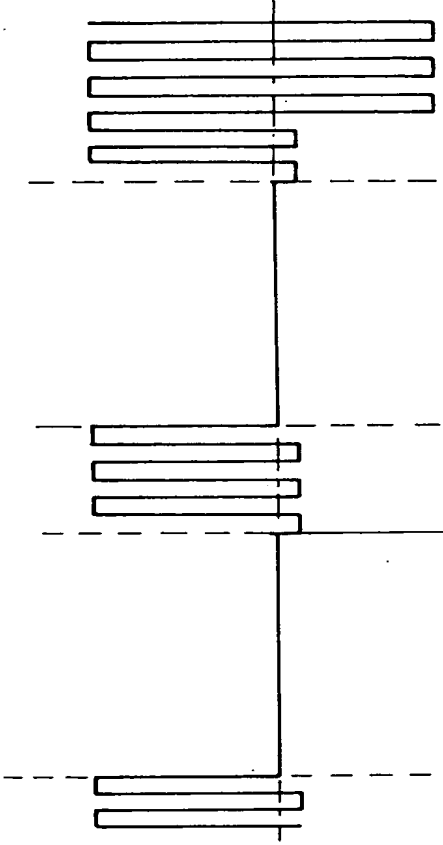


FIG. 12 C
PRIOR ART